AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claims 1-17 (canceled).

Claim 18 (previously presented): A method for manufacturing electronic components, in which conductive pattern layers are laminated to each other with insulating layers provided therebetween to form an integrated laminate, the method comprising the steps of:

alternately laminating the insulating layers and conductive pattern layers including conductive patterns which are formed at intervals therebetween in layer surface directions to form a laminate in which laminate portions of electronic component-forming conductive patterns are collectively formed;

applying a force to the laminate in a lamination direction to form an integrated laminate;

after the force is applied to the laminate in the lamination direction to form the integrated laminate, cutting the laminate along cutting lines provided along boundaries of the laminate portions of the electronic component-forming conductive patterns so as to separate electronic components from each other;

forming at least one removal dummy pattern in at least one of the conductive pattern layers which are to be laminated to each other before one of the insulating layers is provided on a surface of said at least one of the conductive pattern layers, the at least one removal dummy pattern having a size that allows it to be disposed within a cutting-removal region which is a region to be cut and removed by the step of cutting

the laminate;

forming at least one floating dummy pattern in at least one of the conductive pattern layers of the laminate portions of the electronic component-forming conductive patterns so as to be disposed in the vicinity of an outside of the cutting-removal region at an interval therefrom before one of the insulating layers is formed by lamination on a surface of said at least one conductive pattern layer, the at least one floating dummy pattern not being electrically connected to the electronic component-forming conductive patterns; and

the at least one removal dummy pattern is not exposed at end surfaces of separated electronic components.

Claim 19 (previously presented): The method for manufacturing electronic components, according to Claim 18, wherein the at least one floating dummy pattern and the at least one removal dummy pattern are disposed in at least one of the conductive pattern layers so as to be adjacent to each other at an interval therebetween in a layer surface direction of said at least one of the conductive pattern layers, and electronic component-forming conductive patterns of said at least one of the conductive pattern layers, said at least one floating dummy pattern, and said at least one removal dummy pattern are formed from the same material and are also formed in the same step.

Claim 20 (previously presented): The method for manufacturing electronic components, according to Claim 18, wherein one of the conductive pattern layers is provided which does not include the at least one removal dummy pattern at a position which is overlapped with that of the at least one removal dummy pattern of another one of the conductive pattern layers, at least one extension conductor is formed in said one conductive pattern layer from electronic component-forming conductive patterns thereof so as to intersect the cutting-removal region, and said at least one removal dummy

pattern of said another conductive pattern layer and said at least one extension conductor of said one conductive pattern layer are provided at positions which are overlapped with each other.

Claim 21 (previously presented):The method for manufacturing electronic components, according to Claim 18, wherein conductive patterns of one of the conductive pattern layers are provided, said one conductive pattern layer having no floating dummy pattern at a position which is overlapped with that of the at least one floating dummy pattern of another one of the conductive pattern layers, and the at least one floating dummy pattern of said another conductive pattern layer and a portion of the conductive patterns of said one conductive pattern layer are provided at positions which are overlapped with each other.

Claim 22 (previously presented): The method for manufacturing electronic components, according to Claim 20, wherein conductive patterns of one of the conductive pattern layers are provided, said one conductive pattern layer having no floating dummy pattern at a position which is overlapped with that of the at least one floating dummy pattern of another one of the conductive pattern layers, and the at least one floating dummy pattern of said another conductive pattern layer and a portion of the conductive patterns of said one conductive pattern layer are provided at positions which are overlapped with each other.

Claim 23 (previously presented): The method for manufacturing electronic components, according to Claim 18, wherein the conductive pattern layers and the insulating layers are formed using a photolithographic technique.

Claim 24 (previously presented): The method for manufacturing electronic components, according to Claim 18, wherein the electronic component-forming

conductive patterns have a coil pattern shape, and the electronic components are coil components.

Claim 25 (previously presented): A mother substrate for forming many electronic components, comprising:

conductive pattern layers having conductive patterns which are formed at intervals therebetween in layer surface directions; and

insulating layers which are alternately arranged with the conductive pattern layers to form a laminate in which laminate portions of electronic component-forming conductive patterns are collectively provided, the laminate being arranged to be cut along cutting lines provided along boundaries of the laminate portions of the electronic component-forming conductive patterns so as to separate the electronic components from each other; wherein

in at least one of the conductive pattern layers, at least one removal dummy pattern is provided and has a size that allows it to be entirely disposed within a cutting-removal region which is to be cut away along the cutting lines;

in at least one conductive pattern layers of the laminate portions of the electronic component-forming conductive patterns, at least one floating dummy pattern which is not electrically connected to the electronic component-forming conductive patterns is provided in the vicinity of the outside of the cutting-removal region at an interval therefrom; and

the at least one removal dummy pattern is spaced apart from the cutting lines.

Claim 26 (previously presented): The mother substrate for forming many electronic components, according to Claim 25, wherein the at least one floating dummy pattern and the at least one removal dummy pattern are disposed in at least one of the conductive pattern layers so as to be adjacent to each other at an interval therebetween, and electronic component-forming conductive patterns of said at least

one of the conductive pattern layers, said at least one floating dummy pattern, and said at least one removal dummy pattern are formed from the same material.

Claim 27 (previously presented): The mother substrate for forming many electronic components, according to Claim 25, wherein in at least one of other conductive pattern layers having no removal dummy pattern at a position which is overlapped with at least one removal dummy pattern of one of the conductive pattern layers, at least one extension conductor is arranged to extend from electronic component-forming conductive patterns of said at least one of other conductive pattern layers to intersect the cutting-removal region, and said at least one removal dummy pattern of said one conductive pattern layer and said at least one extension conductor of said at least one of other conductive pattern layers are provided at positions which are overlapped with each other.

Claim 28 (previously presented): The mother substrate for forming many electronic components, according to Claim 25, wherein in at least one of other conductive pattern layers having no floating dummy pattern at a position which is overlapped with the at least one floating dummy pattern of one of the conductive pattern layers, a portion of electronic component-forming conductive patterns of said at least one of other conductive pattern layers is disposed at a position which is overlapped with that of said at least one floating dummy pattern of said one conductive pattern layer.

Claim 29 (previously presented): The mother substrate for forming many electronic components, according to Claim 27, wherein in at least one of other conductive pattern layers having no floating dummy pattern at a position which is overlapped with the at least one floating dummy pattern of one of the conductive pattern layers, a portion of electronic component-forming conductive patterns of said at least one of other conductive pattern layers is disposed at a position which is overlapped with

that of said at least one floating dummy pattern of said one conductive pattern layer.

Claim 30 (previously presented): The mother substrate for forming many electronic components, according to Claim 25, wherein the conductive pattern layers and the insulating layers are formed using a photolithographic technique.

Claim 31 (previously presented): The mother substrate for forming many electronic components, according to Claim 25, wherein the electronic component-forming conductive patterns have a coil pattern shape, and the electronic components are coil components.

Claim 32 (currently amended): An electronic component comprising:

conductive pattern layers; and

insulating layers which are alternately arranged with the conductive pattern layers to form a laminate in which the conductive pattern layers are integrally laminated to each other; wherein

in at least one of the conductive pattern layers, at least one floating dummy pattern which is not electrically connected to a corresponding conductive pattern is disposed in a region between an end surface of said at least one of the conductive pattern layers and the conductive pattern at an interval therefrom so as not to be exposed at the end surface of said at least one of the conductive pattern layers; and

no conductive patterns are disposed between ~~the~~ one end surface of ~~said at least one of the conductive pattern layers~~ each of the insulating layers and the at least one floating dummy pattern.

Claim 33 (previously presented): The electronic component according to Claim 32, wherein the conductive pattern layers include extension conductors which extend from the conductive patterns to end surfaces of the conductive pattern layers,

conductive pattern layers having extension conductors provided at positions different from each other are included in the conductive pattern layers, and of the conductive pattern layers having extension conductors provided at positions different from each other, in a region of one of the conductive pattern layers in which no floating dummy pattern is provided and which is overlapped with a region of another one of the conductive pattern layers in which at least one extension conductor is provided, the at least one floating dummy pattern is provided.

Claim 34 (previously presented): The electronic component according to Claim 32, wherein the electronic component-forming conductive patterns have a coil pattern shape, and the electronic component is a coil component.